

1    **WHAT IS CLAIMED IS:**

2    1.    A CMOS structure having a silicon nitride layer in which stress is relaxed by  
3    implantation therein of oxygen-containing or carbon-containing ions.

1    2.    The structure of Claim 1 in which stress is relaxed in a selected area by  
2    preventing ion implantation in all but the selected area.

1    3.    The structure of Claim 2 in which the preventing step is effected by masking all  
2    but the selected area.

1    4.    The structure of Claim 1 in which the stress in the layer is tensile.

1    5.    The structure of Claim 4, which further comprises a PMOS device and an NMOS  
2    device both covered by the layer, and wherein implantation of oxygen-containing or  
3    carbon-containing ions is prevented in the area of the layer overlying the NMOS device.

1    6.    The structure of Claim 1 in which the stress in the layer is compressive.

1    7.    The structure of Claim 6, which further comprises a PMOS device and an NMOS  
2    device both covered by the silicon nitride layer, and wherein implantation of the oxygen-  
3    containing or carbon-containing ions is prevented in the area of the layer overlying the  
4    PMOS device.

1 8. A CMOS structure having a silicon nitride contact etch stop layer overlying one  
2 or more NMOS devices and one or more PMOS devices, comprising:  
3 first areas of the layer overlying one type of device and having oxygen-containing  
4 or carbon-containing ions implanted therein; and  
5 second areas of the layer overlying the other type of device and not having  
6 oxygen-containing or carbon-containing ions implanted therein.

1 9. The structure of Claim 8, wherein the layer is formed by chemical vapor  
2 deposition.

1 10. The structure of Claim 8, wherein the layer is formed by thermal chemical vapor  
2 deposition.

1 11. The structure of Claim 10, wherein:  
2 the first areas overlie the PMOS devices; and  
3 the second areas overlie the NMOS devices.

1 12. The structure of Claim 8, wherein the layer is formed by plasma enhanced  
2 chemical vapor deposition.

1 13. The structure of Claim 12, wherein:  
2 the first areas overlie the NMOS devices; and  
3 the second areas overlie the PMOS devices.

1 14. A method of relaxing stress in a silicon nitride layer of a CMOS structure  
2 comprising implanting oxygen-containing or carbon-containing ions into the layer.

1 15. The method of Claim 14, further comprising preventing oxygen-containing or  
2 carbon-containing ion implantation in all but the selected area of the layer.

1 16. The method of Claim 15, wherein the preventing step is effected by masking all  
2 but the selected area of the layer.

1 17. The method of Claim 14, wherein the stress in the layer is tensile.

1 18. The method of Claim 17, wherein the layer is superjacent to a PMOS device and  
2 to an NMOS device, and further comprising preventing oxygen-containing or carbon-  
3 containing ion implantation into the area of the layer overlying the NMOS device.

1 19. The method of Claim 18, wherein the preventing step is effected by masking all  
2 but the area of the layer overlying the PMOS device.

1 20. The method of Claim 19, wherein the masking step is effected by selectively  
2 applying and developing a photoresist coating on the layer.

1 21. The method of Claim 14, wherein the stress in the layer is compressive.

1 22. The method of Claim 21, wherein the layer is superjacent to a PMOS device and  
2 to an NMOS device, and further comprising preventing oxygen-containing or carbon-  
3 containing ion implantation into the area of the layer overlying the PMOS device.

1    23.    The method of Claim 22, wherein the preventing step is effected by masking all  
2    but the area of the layer overlying the NMOS device.

1    24.    The method of Claim 23, wherein the masking step is effected by selectively  
2    applying and developing a photoresist coating on the layer.

1 25. A method of relaxing the stress in a silicon nitride contact etch stop layer  
2 overlying one or more NMOS devices and one or more PMOS devices, comprising:  
3 selectively implanting oxygen-containing or carbon-containing ions into areas of  
4 the layer overlying one type of device; and  
5 simultaneously preventing implantation of the ions into areas of the layer  
6 overlying the other type of device.

1 26. The method of Claim 25, wherein the preventing step is effected by masking the  
2 areas of the layer overlying the other type of device.

1 27. The method of Claim 26, wherein the masking step is effected by selectively  
2 applying and developing a photoresist coating on the layer.

1 28. The method of Claim 25, wherein the layer is formed by chemical vapor  
2 deposition.

1 29. The method of Claim 25, wherein the layer is formed by thermal chemical vapor  
2 deposition.

1 30. The method of Claim 29, wherein the developed photoresist masks the NMOS  
2 devices.

1 31. The method of Claim 25, wherein the layer is formed by plasma enhanced  
2 chemical vapor deposition.

1     32.    The method of Claim 31, wherein the developed photoresist masks the PMOS  
2    devices.